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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,919	12/24/2003	Hisashi Ishikawa	Q79066	9181

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EXAMINER	
HUR, JUNG H	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,919	ISHIKAWA, HISASHI	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/24/03, 8/17/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

1. Claims 1-20 are pending in the application.

Information Disclosure Statement

2. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 24 December 2003 and 17 August 2005. The information disclosed therein was considered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Delp et al. (U.S. Pat. No. 6,334,174) in view of Ozawa et al. (U.S. Pat. No. 6,483,772) and Solomon et al. (U.S. Pat. No. 6,681,293).

Regarding claim 1, Delp, for example in Figs. 5-7, discloses a semiconductor memory device comprising: a memory (76 in Fig. 5); and a memory control circuit (78 in Figs. 5 and 6) for controlling said memory, wherein: said memory control circuit includes: a bank busy circuit for variably setting a bank busy time that controls different bank cycle times (related to, for example, "bank cycle time"; see column 7, lines 5-19 and Figs. 6 and 7); a read data input circuit for inputting read data output from said memory in variable input timing (see column 7, lines 5-

19 and Figs. 6 and 7 for various timing parameters); a write data output circuit for outputting write data to said memory in variable output timing (see column 7, lines 5-19 and Figs. 6 and 7 for various timing parameters); a command control circuit for issuing a command to said memory based on a memory command output from said bank busy circuit (for example, via 96 in Fig. 7), thereby controlling different command interfaces (via, for example, 82a and 82); and an address generation circuit for controlling different address interfaces (88 through 82a, 82 and 84 in Fig. 6), and said memory control circuit controls different memories using the same hardware (see for example column 10, lines 42-54 and column 11, lines 7-15).

Delp does not disclose a write mask circuit for controlling different write masks; and an initial sequence control circuit for controlling memories different in the initial sequence.

Ozawa discloses a write mask circuit for controlling different write masks (Data Mask method and Variable Write burst length method; see for example column 1, lines 34-36, column 2, lines 4-22, and column 8, lines 39-47).

Solomon discloses an initial sequence control circuit for a memory (see for example column 27, line 39 through column 28, line 15).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include, in the device of Delp, a write mask circuit for controlling different write masks (as in Ozawa), for the purpose of providing a greater flexibility in accommodating additional types of memories, including high-speed memories, such as FCRAMs and DDRIIs (see for example Ozawa column 2, lines 4-14).

Further, since it was common and well known in the art to initialize a memory through an initial command sequence that would be unique to the memory (as exemplified in Solomon), it

would have been obvious at the time the invention was made to a person having ordinary skill in the art to additionally include, in the device of Delp, an initial sequence control circuit for controlling memories different in the initial sequence, for the purpose of reliably initializing a selected type of memory among various memory types.

Regarding claims 2 and 4, the above Delp/Ozawa/Solomon combination further discloses that: said bank busy circuit includes: a program register (94 in Figs. 6 and 7 of Delp) for variably setting the bank busy time; and a bank busy counter (98d in Fig. 7 of Delp) for setting a value set on said program register, and then counting down the set value for each clock cycle when a bank n is accessed for turning on, and said bank busy circuit provides said command control circuit with a memory command indicating cleared bank busy when the logic value of said bank busy counter becomes zero, thereby controlling memories different in the bank cycle time (see for example Delp column 12, lines 10-26 and 58-60);

wherein said bank busy circuit switches the bank busy time using a switch (see for example 84 in Fig. 6 and 98d in Fig. 7 of Delp).

Regarding claim 3, the above Delp/Ozawa/Solomon combination further discloses that: said read data input circuit includes a first program register (as a part of 94 in Fig. 6 of Delp) for variably setting the input timing of the read data output from said memory for controlling memories different in the access time, and inputs the read data output from said memory based on a set value on the first program register in variable input timing, and said write data output circuit comprises a second program register (as a part of 94 in Fig. 6 of Delp) for variably setting

the output timing of the write data output to said memory, and adjusts the write data output timing based on a set vale on the second program register (see for example Delp column 7, lines 5-19 and Figs. 6 and 7 for various timing parameters).

Regarding claims 5 and 6, the above Delp/Ozawa/Solomon combination further discloses that: said write mask circuit relates to mask control for the write data output to said memory, and has a program register (94 or 92, as modified in the above Delp/Ozawa/Solomon combination) or a switch (84, as modified in the above Delp/Ozawa/Solomon combination) for switching between masking write operation using a Variable Write function when an FCRAM or an NWRAM is used, and masking the write operation using a Data Mask function when a DDR-SDRAM is used (see for example Ozawa column 2, lines 4-14, wherein DDR-SDRAM is distinguished from DDRIIs or DDR2s).

Regarding claims 7 and 8, the above Delp/Ozawa/Solomon combination further discloses that: said address generation circuit (88 in Fig. 6 of Delp) relates to address generation of memories different in address assignment (controlled by registers 90; see Fig. 6), and includes a program register (94 in Fig. 6) or a switch (84 in Fig. 6) for switching address generation logic (via 82 and 82a in Fig. 6).

Regarding claims 9 and 10, the above Delp/Ozawa/Solomon combination further discloses that: said initial sequence control circuit relates to control of memories different in the initial sequence, includes a program register (94 or 92, as modified in the above

Delp/Ozawa/Solomon combination) or a switch (84, as modified in the above Delp/Ozawa/Solomon combination) for variably changing the issue sequence of commands including mode register set (MRS), extension mode register set (EMRS), auto refresh, and all bank pre-charge, and for variably changing set values on a mode register and an extension mode register, controls said memories different in the initial sequence using the same circuit, and issues an initial sequence command including the mode register set (MRS), the extension mode register set (EMRS), the auto refresh, and the all bank pre-charge to said command control circuit (see for example Solomon column 27, line 39 through column 28, line 9).

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Delp et al. in view of Ozawa et al. and Solomon et al. as applied to claim 1 above, and further in view of Chang (U.S. Pat. No. 6,621,754)

The above Delp/Ozawa/Solomon combination discloses a semiconductor memory device as recited in claim 1, with the exception of a power supply capable of adjusting a power supply output level supplied for said memory.

Chang discloses a memory device comprising a power supply capable of adjusting a power supply output level supplied for a memory (see for example column 1, lines 59-67).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include, in the device of the Delp/Ozawa/Solomon combination, a power supply capable of adjusting a power supply output level supplied for the memory (as in Chang), for the purpose of providing a greater flexibility in accommodating additional types of memories requiring different supply voltages (see for example Chang column 1, lines 59-67).

6. Claims 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Delp et al. in view of Ozawa et al. and Solomon et al. as applied to claims 1-3 above, and further in view of Doyle (U.S. Pat. No. 5,982,655).

The above Delp/Ozawa/Solomon combination discloses a semiconductor memory device as recited in claims 1-3, with the exception of a mount-type semiconductor device for mounting said semiconductor memory device on a board, wherein: said memory is different in the package size or the pin assignment, only the board for mounting the memory is changed, and one type of mother board is used for connecting the board for mounting the memory thereon when the memory different in the package size or the pin assignment is mounted; and wherein the board for mounting the memory thereon is a DIMM (Dual Inline Memory Module).

Doyle discloses a mount-type semiconductor device for mounting said semiconductor memory device on a board (DIMM; see for example column 2, lines 9-15), wherein: said memory is different in the package size or the pin assignment, only the board for mounting the memory is changed, and one type of mother board is used for connecting the board for mounting the memory thereon when the memory different in the package size or the pin assignment is mounted (see for example column 2, lines 9-15).

Since a DIMM configuration was common and well known in the art (as exemplified in Doyle), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to include, in the device of the Delp/Ozawa/Solomon combination, a means to support memories with different package sizes or pin assignments on a DIMM (as in Doyle), for the purpose of providing a greater flexibility in accommodating additional types of

memories with various packages sizes or pin assignments (see for example Doyle column 2, lines 9-15).

7. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Delp et al. in view of Ozawa et al. and Solomon et al. as applied to claims 1-3 above, and further in view of Park et al. (U.S. Pat. No. 6,480,409).

The above Delp/Ozawa/Solomon combination discloses a semiconductor memory device as recited in claims 1-3, with the exception of a mount-type semiconductor device for mounting said semiconductor memory device on a board, wherein: said memory is different in whether a terminating resistor is incorporated or not, and when the memory which is different in whether a terminating resistor is incorporated or not is mounted, a terminating resistor is not mounted on a DIMM (Dual Inline Memory Module) for the memory incorporating a terminating resistor, and a terminating resistor is attached to a DIMM for the memory not incorporating a terminating resistor, and one type of mother board is provided for connecting to the board for mounting the memory thereon.

Park disclose a memory device and a terminating resistor mounted on a DIMM (see for example Figs. 3, 4 and 7).

Since use of terminating resistors was common and well known in the art (as exemplified in Park), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to mount a terminating resistor on a DIMM for memories that do not incorporate a terminating resistor while not mounting a terminating resistor for memories that do incorporate a terminating resistor, for the purpose of ensuring reduced noise and improved signal

quality in a memory device that supports various types of memories, including those with or without a terminating resistor.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

9/2/05

J. H. Hur
Patent Examiner
Art Unit 2824

jhh